REMARKS/ARGUMENTS

Claims 1-5 and 10-15 are pending in this application. Claims 3 and 18 have been canceled without prejudice or disclaimer. Claims 1, 2, 4 and 5 have been amended. No new matter has been added. Claims 6-9 and 16-17 have been withdrawn from consideration by the Examiner.

DRAWINGS

Applicants submit herewith a replacement sheet of the drawing for Fig. 48 with the legend PRIOR ART, as required. In view of the cancellation of claim 18, which has been canceled without prejudice or disclaimer, the drawings should be accepted as filed, and therefore no changes to the drawings, other than to Fig. 48, should be required. Accordingly, the objection to the drawings should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §§102 AND 103

Claims 1 and 3-5 are rejected under 35 U.S.C. §102(e) as being anticipated by Horii, U.S. Patent Application Publication No. 2003/0209746. Claim 2 is rejected under 35 U.S.C. §103(a) as being unpatentable over Horii, U.S. Patent Application Publication No. 2003/0209745 in view of Kuge, U.S. Patent No. 6,597,031; and also over Johnson et al., U.S. Patent Publication No. 2005/0030800 (Johnson) in view of Horii. Further, claims 10-15 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Horii in view of Johnson. Applicants request reconsideration of these rejections for the following reasons.

The semiconductor integrated circuit of the present invention includes a second electrode layer film that is provided on the upper part of a phase change material layer film in combination with memory cells made up by electrically connecting a resistor and a field effect transistor. Further, according to the present invention, the upper part of the phase change material layer film can be covered by providing the second electrode layer film to a plurality of memory cells in common. Consequently, the second electrode layer film can protect the phase change material layer film from deterioration of the device due to processing.

The semiconductor integrated circuit of the present invention provides a stacked layer having a phase change material layer film and a second electrode layer film, whereas as shown in Fig. 6 of Horii, a plate electrode 83 is connected to a phase change material layer 71. Thus, the semiconductor integrated circuit of the invention differs from that of Horii. That is, the composition of Horii may cause a deterioration of the device due to processing because an additional process step is required to make a hole of an oxidation resistant layer 73, and the phase change material layer 71 may then be exposed. Further, the invention of Horii shows in Fig. 2A that a phase change region 71a is provided on the upper part of the phase change material layer. Accordingly, the hole must be formed in the upper part of the phase change material layer. Thus, the Horii structure differs from the present invention which protects the phase change material layer film. Accordingly, the disclosure of Horii does not anticipate the invention as set forth in claims 1 and 3-5 and, therefore, the 35 U.S.C. §102(e) rejection should be withdrawn.

Kuge is relied upon for disclosing a semiconductor integrated circuit having a plurality of memory cells. However, Kuge differs from the present invention in that Kuge discloses vertical bipolar transistors. The Office Action states that Kluge discloses that the stacked resistor elements to be connected in common may result in high integration. However, this is a misinterpretation of the reference since the means to realize the high integration is the vertical bipolar transistor. See the description in Kuge, column 7, line 40 which discusses that the bipolar transistors 101a to 101c and 102a to 102c are of a so-called vertical bipolar type, which are laminated in a vertical direction. Therefore, a plurality of the bipolar transistors 101a to 101c can be formed in a small area. As a result, the degree of integration of the semiconductor memory devices 351 can be enhanced. Further, the reason why the stacked resistor elements are to be connected in common is to use the stacked resistor elements as a bit line (see col. 6, line 12 of Kuge). Accordingly, the combination of Horii and Kuge does not render the invention as set forth in claim 2 unpatentable under 35 U.S.C. §103(a).

In Johnson, only one memory device is disclosed even though the Office Action states that the reference discloses a plurality of memory devices. No description is provided in Johnson of a second electrode layer film which is required in the present invention and which is

provided to the plurality of memory cells, in common. In the combination of Horii and Johnson, there is no disclosure of a second electrode layer as in the present invention, which is stacked on a phase change material film, and provided to a plurality of memory cells in common. Thus, the combination of Horii and Johnson does not render the invention as set forth in claims 2 and 10-15 unpatentable under 35 U.S.C. §103(a) and the rejection should be withdrawn.

CONCLUSION

In view of the foregoing, Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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